A MONOLITHIC HIGH POWER Ka BAND PIN SWITCH

J. V. Bellantoni, D. C. Bartle, D. Payne, G. McDermott
S. Bandla, R. Tayrani, and L. Raffaelli

GAMMA MONOLITHICS
A partnership between Martin Marietta Corp. and Alpha Industries Inc.
20 Sylvan Rd.
Woburn, MA 01801

Abstract—A high power Ka Band SPDT switch using monolithic GaAs epitaxial PIN diode technology is presented. Insertion loss is 0.7 dB at 35 GHz, and isolation is better than 32 dB from 30 to 40 GHz. The power handling capability is at least + 38 dBm pulsed and +35 dBm CW. Switching speed rise and fall times are 2 ns.

Introduction

The degree to which a millimeter–wave radar system can accurately locate a moving object is, in large part, dependent upon the RF transceiver section of the system. The transceiver performs the important function of interfacing computer proccesing and control with the transmitted and reflected radar signals. One of the more fundamental functions of a transceiver is to route signals from the antenna to the transmitter or receiver. The RF switch employed for this purpose should have low insertion loss and high power handling capabilities. A low loss, high power switch in the RF transeiver section is essential to realize the full potential of a millimeter–wave system.

In this paper we describe the development and testing of a monolithic SPDT switch designed to meet the progressively increasing power requirements of developing millimeter–wave systems. Previous work has been reported on monolithic switch circuits employing planar PIN structures [1,2] or MESFET devices [3]. The switch presented here employs epitaxial vertical PIN diode structures [4] in a shunt configuration optimized for low loss and high isolation under high power signal conditons. The vertical epitaxial structure is expected to provide lower RF impedance under foward bias than planar ion implanted PIN structures [5] and superior power handling capablity than MESFETs. An additional feature of the circuit described here is the location of the PIN diode directly underneath the RF line. This can improve isolation and increase bandwidth compared to planar devices, which are neccessarily positioned adjacent to, or a quarter–wave from, the RF line.

Circuit Description

Figure 1 is a schematic illustration of a typical computer model employed for design and analysis. Each output arm contains a PIN diode spaced a quarter–wavelength from the common input arm. When foward biased, the low impedance PIN diode is transformed through the quarter-wave section to present a high impedance at the switch junction. Simultaneously, the junction capacitance of the reverse biased PIN in the second arm is tuned to a low-pass filter response by the inductive air bridge interconnects.

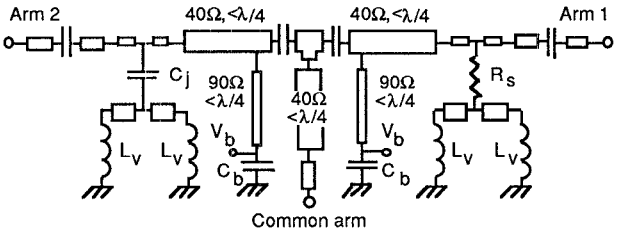

Figure 1. Computer model of a prototype SPDT switch structure. Arm 1 is in the isolation state, arm 2 is in the loss state.

Insertion losses associated with the prototype design can be optimized by properly selecting the elements for a low ripple Tchebysheff response. Analysis by computer predicts that most of the critical dimensions in the circuit depend upon the diode parameters. In order to reduce the amount of empirical work required to characterize the diode, a theoretical investigation was conducted to determine R_s and C_j as a function of the structure dimensions. The design curves generated from the computations were used in conjunction with computer analysis to identify possible diode structures that meet specified performance requirments. A simple thermal analysis and voltage breakdown calculation was also included to insure that the diodes selected would survive under high power conditions.

Several different circuit configurations have been investigated and are presented in [6]. A photograph of the switch described here is shown in Fig. 2. Via holes are used to ground each diode and form coplanar probe pads at the RF input and output ports. Parasitic capacitances are minimized by champhoring the RF line near via holes. The chip measures 1.9 x 3.4 mm (76 x 136 mils).

Bias is applied to the two pads near the top edge of the chip. The MIM capacitor, C_b, used in the bias filter conserves space and eliminates any bias port isolation problems that may occur with radial stubs. The bias lines have been placed on the chip above the output arms (see Fig. 2). This simplifies the machining of bias channels in a test fix-

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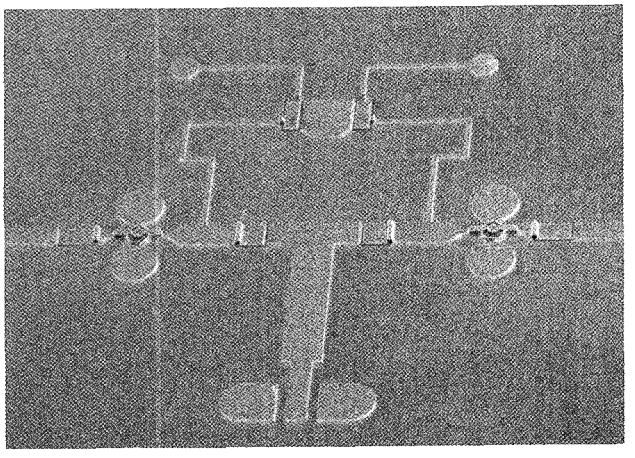


Figure 2 SEM photograph of the Ka band switch.

ture. The chip size can be significantly reduced by placing the bias lines in the regions below the output arms. Such a bias configuration would be suitable for an integrated application where the chip is bonded directly to other monolithic circuits.

GaAs PIN Diode

A SEM photograph of the double mesa structure is shown in Fig. 3. The vertical epitaxial structure employed minimizes intrinsic resistance and increases carrier injection efficiency as compared to a planar structure [6]. The diode has a 0.4 μm thick p^+ top layer with a free hole concentration of 2 x 10^{19} cm^{-3} followed by a 3 μm thick intrinsic layer of 1 x 10^{15} cm^{-3} n-type material and a 4 μm, 2 x 10^{18} cm^{-3} n^+ bottom layer. The diode has a C_j of 65 fF at -5 V reverse bias and R_s of 1.5 Ω at +30 mA foward bias.

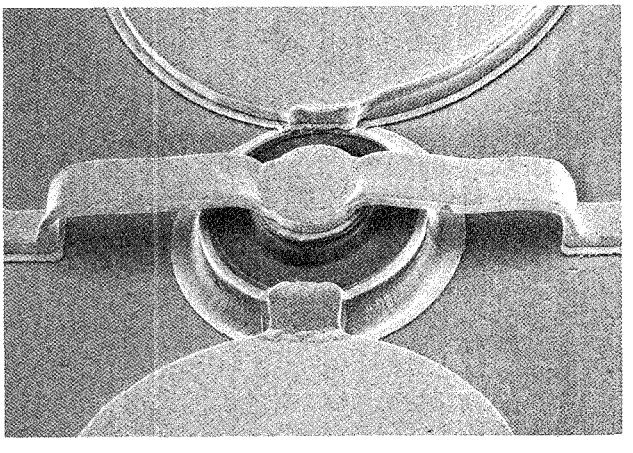


Figure 3 SEM photograph of the vertical PIN diode.

Fabrication

The PIN structures were grown by MOCVD on LEC semi-insulating GaAs substrates. Isotropic etching was used to fabricate the circular double mesa structure. Au/Ag/Zn and AuGe/Ni/Au evaporated films were alloyed into the p^+ and n^+ terminals respectively to form ohmic contacts. Evaporation and lift off were used to define transmission lines and DC bias pads. Diode passiviation and dielectric layers for MIM capacitors were produced by PECVD of Si_3N_4 and plasma etching. Electroplating of transmission lines and air bridges completed front side wafer processing. After lapping and polishing the wafer to 100 μm, via holes were etched from the backside by reactive ion etching. Backside metalization and plating provided the ground plane. Street etching and chip seperation completed the process.

Experimental Results

Figure 4 is a photograph of the test fixture used for high power testing. The quartz microstrip boards that interconnect the chip with the coax-to-microstrip transitions are recessed in channels to enhance arm to arm isolation. Bias pins can been seen at the front of the fixture. The fixture has 1.1 dB loss and 22 dB of return loss at the test frequency of 35 GHz.

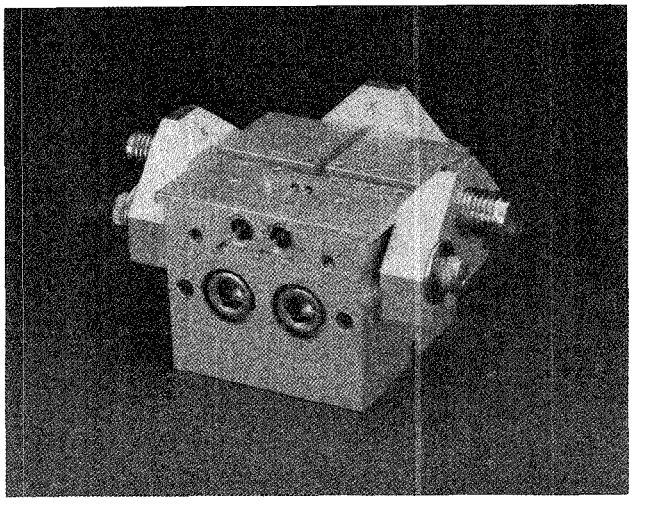


Figure 4 Microstrip test fixture for high power testing.

The essential details of the high power measurment system are illustrated in Fig. 5. A pulsed Impatt source supplied +38 dBm to the device under test with a pulse width of roughly 100 ns. A sweep generator and TWT amplifier provided +35 dBm for the CW test. These power levels were the maximum possible with the available test equipment. Insertion loss and isolation were monitored using power meters. Bias for the arm in isolation was held at +25 mA during the 40 minute testing intervals. Initially the bias for the low loss arm was set to -5 volts. However the bias level had to be increased to more than -15 volts during high power testing to maintain minimum insertion loss. The increased bias level was necessary to prevent charge injected into the I region during foward-going RF voltage excursions from multiplicatively increasing through

impact ionization with each succeeding RF cycle[7]. Degradation in performance was not observed after the bias level was adjusted and the results of a small signal RF evaluation were identical, within expermental error, to previously recorded data.

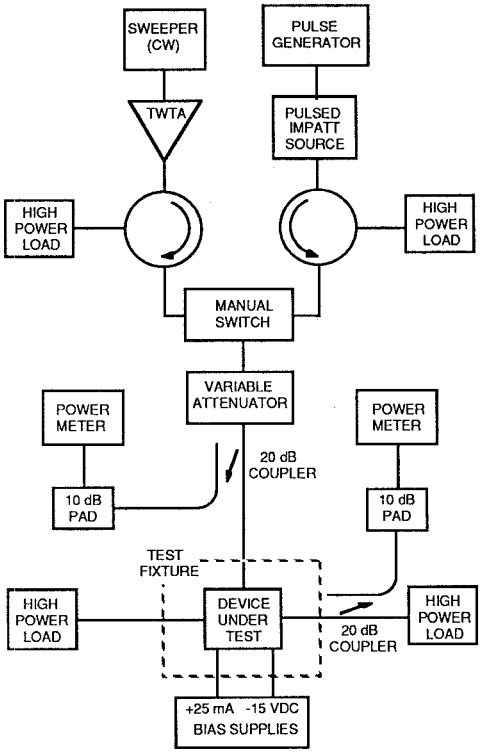


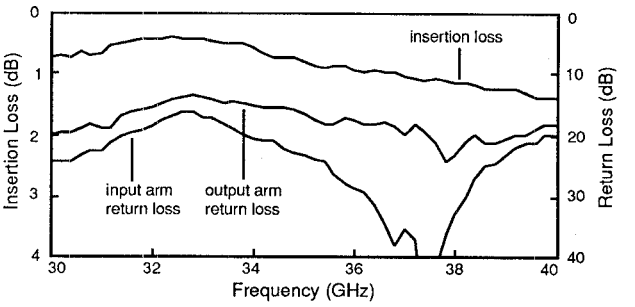
Figure 5 High power test stand block diagram.

Wafer evaluation used a coplanar waveguide probe station and an automated vector network analyzer. Results are shown in Fig. 6. Insertion loss is 0.7 dB at 35 GHz. Isolation is better than 32 dB from 30 to 40 GHz. The return loss of the common arm is better than 40 dB (1.05:1 VSWR) at 37.5 GHz, indicating that some circuit parameters should be adjusted slighty to center the response.

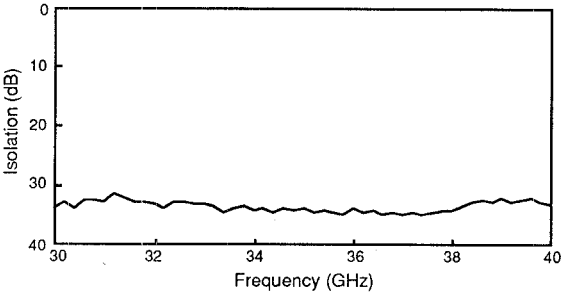
Switching speed measurments are presented in Fig. 7. The 10 to 90% RF and 90 to 10% RF rise and fall times are 2 ns. The 50% TTL to 90% RF and 50% TTL to 10% RF are 10 ns. The Alpha 66245 inverting driver that applied +10 mA and -12 volts to the switch has a 7 ns delay between the 50% TTL and 50% output drive levels.

Conclusion

The monolithic Ka band PIN diode switch described here has demonstrated excellent RF characteristics under high power conditions. Insertion loss is 0.7 dB at 35 GHz and isolation is better than 32 dB from 30 to 40 GHz. The switch is capable of handling +38 dBm pulsed and +35 dBm CW, which were the maximum power rating of the test equipment available. Switching speed is 2 ns.

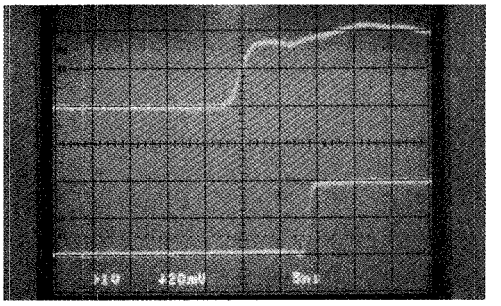


(a)

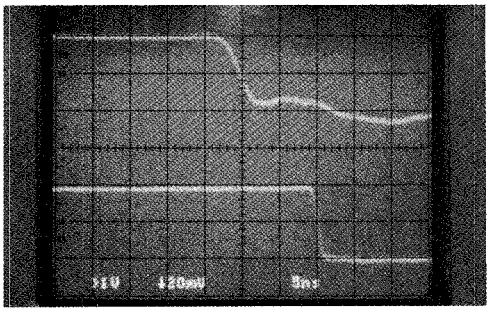


(b)

Figure 6 On wafer probe measurments: (a) insertion loss characteristics and (b) isolation of the switch. Bias is - 5 volts and + 15 mA.



(a)



(b)

Figure 7 (a) Measured OFF to ON time and (b) ON to OFF time of the switch. Upper traces are TTL signals, lower traces are detected RF signals. The horizontal axis is 5 ns per division.

Acknowledgements

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